AMENDMENTS TO THE CLAIMS

Claim listing:

1. (Currently Amended) A line decoder for a memory cell responsive to an address comprising:

a. a synchronous portion disposed to receive and respond to a clocked signal;

b. an asynchronous portion coupled with a line for the memory cell; and

c. a feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion and resetting the decoder in response to an asynchronous reset signal independent of the clocked signal.

2. (Previously Presented) The decoder of Claim 1, wherein the feedback-resetting portion substantially isolates the synchronous portion from the asynchronous portion responsive to a monitor signal.

3. (Canceled)

4. (Currently Amended) The decoder of Claim 1, wherein the decoder ~~is~~ comprises an asynchronously-resettable row decoder.

5. (Canceled)

6. (Currently Amended) A decoder in a memory module ~~having~~ including a plurality of memory cell groups, comprising:

a. a signal input;

b. a first memory output coupled with a first memory cell group;

c. a second memory output coupled with a second memory cell group; and

d. a selector coupled between the signal input, the first memory output, and the second memory output, wherein in the event of a fault detected on the first memory output when the decoder is in service, the decoder decodes an address to enable the second memory cell group responsive to a group-select signal.

7. (Previously Presented) The decoder of Claim 6, wherein the selector comprises a multiplexer, the multiplexer selecting to decode from one of the first memory cell group and the second memory cell group, the multiplexer being responsive to the group-select signal.

8. (Currently Amended) The decoder of Claim 6, wherein the decoder ~~is~~ comprises a row decoder disposed in a memory module having a plurality of adjacent memory rows, and wherein a first memory row and a second memory row ~~are~~ comprise the adjacent memory rows in the memory module, and the group-select signal ~~is~~ comprises an alternative-row-select signal.

9. (Currently Amended) The decoder of Claim 6, wherein the decoder ~~is~~ comprises a column decoder disposed in a memory module having a plurality of adjacent memory columns, and wherein a first memory column and a second memory column ~~are~~ comprise the adjacent memory columns in the memory module, and the group-select signal ~~is~~ comprises an alternative-column-select signal.

10. (Currently Amended) The decoder of Claim 6, wherein the decoder ~~is~~ comprises a row decoder disposed in a memory module having assigned memory rows and a redundant memory row, and wherein ~~the~~ a first memory row ~~is an~~comprises one of the assigned memory ~~row~~rows, ~~the~~ a second memory row ~~is~~ comprises the redundant memory row and the group-select signal ~~is~~ comprises a redundant-row-select signal.

11. (Canceled)

12. (Currently Amended) A decoder in a memory module ~~having~~ including a plurality of memory cell groups, comprising:

a. a synchronous portion, disposed to receive and respond to a clocked signal;

b. an asynchronous portion, coupled with a selected memory cell group;

c. a feedback-resetting portion comprising an input receiving an input signal from the asynchronous portion and an output transmitting an output signal to the synchronous portion in response to the input signal, the feedback-resetting portion substantially isolating the synchronous portion from the asynchronous portion responsive to an asynchronous reset signal;

d. a signal input;

e. a first memory output coupled with a first memory cell group;

f. a second memory output coupled with a second memory cell group; and

g. a selector coupled between the signal input, the first memory output, and the second memory output, wherein in the event of a fault detected on the first memory output when the decoder is in service, the decoder decodes an address to enable the second memory cell group responsive to a group-select signal.

13. (Previously Presented) The decoder of Claim 12, wherein the selector comprises a multiplexer, the multiplexer enabling one of the first memory cell group and the second memory cell group in response to the group-select signal.

14. (Currently Amended) The decoder of Claim 12, wherein the decoder ~~is~~ comprises a row decoder disposed in a memory module ~~having~~including a plurality of adjacent memory rows, and wherein a first memory row and a second memory row ~~are~~ comprise the adjacent memory rows in the memory module, and the group-select signal ~~is~~ comprises an alternative-row-select signal.

15. (Currently Amended) The decoder of Claim 12, wherein the decoder ~~is~~ comprises a column decoder disposed in a memory module ~~having~~ including a plurality of adjacent memory columns, and wherein a first memory column and a second memory column ~~are~~ comprise the adjacent memory ~~column~~columns in the memory module, and the group-select signal ~~is~~ comprises an alternative-column-select signal.

16. (Currently Amended) The decoder of Claim 12, wherein the decoder ~~is~~ comprises a row decoder disposed in a memory module ~~having~~ including assigned memory rows and a redundant memory row, and wherein ~~the~~ a first memory row ~~is an~~ comprises one of the assigned memory ~~row~~rows, ~~the~~ a second memory row ~~is~~

comprises the redundant memory row and the group-select signal ~~is~~ comprises a redundant-row-select signal.

17. (Canceled)